UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,230	04/08/2004	Mark B. Fuselier	2000.092182	9406

23720 7590 06/06/2005

WILLIAMS, MORGAN & AMERSON, P.C.
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

EXAMINER	
KANG, DONGHEE	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,230	FUSELIER ET AL.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 49-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 49-73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **1-5, 7-11, 13-16, 18-21, 23-25, 27-29 & 49-66** are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (US 6,441,436).

Re claims **1-3, 8-9, 13-14, 19, 23, 49-50, 52, 56-58, 60, & 62-66**, Wu et al. teach a transistor comprised a channel region, said transistor, comprising (Fig.9):

a bulk silicon substrate (103); a multiple thickness buried oxide layer (104 & 212a) formed above said bulk substrate, said bulk buried oxide layer comprising a substantially planar upper surface, a first section positioned between the two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second section; an active layer (101a) formed above said buried oxide layer, said active layer having a substantially planar lower surface, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer; and a doped back

gate region (101b) positioned at least partially in said bulk substrate under said multiple thickness buried oxide layer. See also Col.2, line 58 – Col.5, line 11.

Re claims **4, 15, 24, & 51**, Wu et al. teach said transistor is part of at least one of a microprocessor, a memory device and a logic device.

Re claims **5, 16, & 25**, Wu et al. teach said active layer is comprised of silicon.

Re claims **7, 18, & 27**, Wu et al. teach said buried oxide layer is comprised of silicon dioxide.

Re claims **10-11, 20-21, 28-29, 53-55, 59, & 61**, Wu et al. teach said transistor comprised of a gate electrode (122), said first section being at least partially positioned under said gate electrode or said first section being substantially aligned with said gate electrode.

3. Claim **55** is rejected under 35 U.S.C. 102(e) as being anticipated by Riccobene (US 6,515,333)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Riccobene teaches a semiconductor device, comprising (Fig.1):

a bulk substrate (18); a buried oxide layer (16) formed above said bulk substrate, said buried oxide layer comprising a first section positioned between the two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second section, said first section being substantially aligned with a gate electrode of said transistor; and an active layer (14) formed above said buried oxide layer, said transistor formed in said active layer above said buried oxide layer. See also Col.3, lines 13-32.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **6, 17, 26, 67-68, 69 & 72** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US 6,441,436) in view of Shigyo et al. (US 5,760,442).

Re claims 6, 17, 26, 67-68 & 72, Wu et al. teach a thickness of active layer is approximately 1 micrometer but from approximately 5 to 30 nm. Shigyo et al teach the active layer has a 25 nm thickness (Col.8, lines 35-40). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the thickness of said active layer having 25 nm as taught by Shigyo in Wu's device, since it has been held that where the general conditions of a claim are disclosed in the

prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Re claim **69**, Wu et al. teach said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is substantially aligned with said gate electrode.

6. Claims **12, 22, 30, 70-71 & 73** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (6,441,436).

Wu et al. teach said first section having a thickness ranging from 5-40 nm but said section having a thickness ranging from approximately 120-180 nm. Although Riccobene does not explicitly teach the thickness raging from 120 ~ 180 nm, it is an obvious matter of routine experimentation to find the optimal thickness ranges. Generally, difference in thickness will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such thickness is critical.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to select the thickness of the active layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Response to Arguments

7. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments filed 04-04-05 have been fully considered but they are not persuasive.

Applicant argues that Riccobene does not teach that the first section of buried oxide layer is substantially aligned with the gate electrode of the transistor. This is not convincing. Claim 55 recites said first section being **substantially** aligned with a gate electrode of said transistor. Indeed, the Federal Circuit recently recognized that, for example, "substantially flattened surface" covered both perfectly flattened surfaces and surfaces with some degree of curvature. See Playtex Prods., Inc. v. Procter & Gamble Co., 2005 U.S.App. Lexis 3693, *22-23 (Fed Cir. March 7, 2005). The first section does not have to be perfectly aligned with the gate electrode of transistor.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang, Ph.D.
Primary Examiner
Art Unit 2811

dhk